

wherein said semiconductor island of p-channel thin film transistor has a hole mobility in the range of $10 \text{ cm}^2/\text{V}\cdot\text{sec}$ or more and said semiconductor island of n-channel thin film transistor has an electron mobility in the range of $15 \text{ cm}^2/\text{V}\cdot\text{sec}$ or more,

wherein at least one of said semiconductor islands comprises boron at a concentration in the range of 1×10^{15} to $1 \times 10^{18} \text{ cm}^{-3}$, and

wherein each of said semiconductor islands has a thickness in the range of 5000 \AA or less.

22. (Amended) A semiconductor circuit having a pixel portion and a shift register, said shift register including at least one pair of complementary p-channel and n-channel thin film transistors, and said pixel portion including at least one thin film transistor, each of said transistors comprising:

a crystalline semiconductor island on an insulating surface, said semiconductor island having source and drain regions and a channel region;

a gate insulating film adjacent to at least said channel region;

a gate electrode adjacent to said gate insulating film; and

a leveling film covering each of said thin film transistors in both of the pixel portion and the shift register,

wherein said semiconductor island of p-channel thin film transistor has a hole mobility in the range of $10 \text{ cm}^2/\text{V}\cdot\text{sec}$ or more and said semiconductor island of n-channel thin film transistor has an electron mobility in the range of $15 \text{ cm}^2/\text{V}\cdot\text{sec}$ or more,

wherein at least one of said semiconductor islands comprises boron at a concentration in the range of 1×10^{15} to $1 \times 10^{18} \text{ cm}^{-3}$, and

wherein each of said semiconductor islands has a thickness in the range of 5000 \AA or less.

23. (Amended) A semiconductor circuit having a pixel portion and an inverter, said inverter including at least one pair of complementary p-channel and n-channel thin film transistors, and said pixel portion including at least one thin film transistor, each of said transistors comprising:

a crystalline semiconductor island on an insulating surface, said semiconductor island having source and drain regions and a channel region;

a gate insulating film adjacent to at least said channel region;

a gate electrode adjacent to said gate insulating film; and
a leveling film covering each of said thin film transistors in both of the pixel portion and the inverter,

wherein said semiconductor island of p-channel thin film transistor has a hole mobility in the range of $10 \text{ cm}^2/\text{V}\cdot\text{sec}$ or more and said semiconductor island of n-channel thin film transistor has an electron mobility in the range of $15 \text{ cm}^2/\text{V}\cdot\text{sec}$ or more,

wherein at least one of said semiconductor islands comprises boron at a concentration in the range of 1×10^{15} to $1 \times 10^{18} \text{ cm}^{-3}$, and

wherein each of said semiconductor islands has a thickness in the range of 5000 \AA or less.

24. (Amended) A semiconductor circuit having a pixel portion and a clocked inverter, said clocked inverter including at least one pair of complementary p-channel and n-channel thin film transistors, and said pixel portion including at least one thin film transistor, each of said transistors comprising:

a crystalline semiconductor island on an insulating surface, said semiconductor island having source and drain regions and a channel region;

a gate insulating film adjacent to at least said channel region;

a gate electrode adjacent to said gate insulating film; and

a leveling film covering each of said thin film transistors in both of the pixel portion and the clocked inverter,

wherein said semiconductor island of p-channel thin film transistor has a hole mobility in the range of $10 \text{ cm}^2/\text{V}\cdot\text{sec}$ or more and said semiconductor island of n-channel thin film transistor has an electron mobility in the range of $15 \text{ cm}^2/\text{V}\cdot\text{sec}$ or more,

wherein at least one of said semiconductor islands comprises boron at a concentration in the range of 1×10^{15} to $1 \times 10^{18} \text{ cm}^{-3}$, and

wherein each of said semiconductor islands has a thickness in the range of 5000 \AA or less.

25. (Amended) An active matrix display device having a pixel portion and a driver circuit portion, said driver circuit portion including at least one pair of complementary p-channel and n-channel thin film transistors, and said pixel portion including at least one thin film transistor, each of said transistors comprising:

a crystalline semiconductor island on an insulating surface, said semiconductor island having source and drain regions and a channel region;

a gate insulating film adjacent to at least said channel region; and a gate electrode adjacent to said gate insulating film; and

a leveling film covering each of said thin film transistors in both of the pixel portion and a part of the driver circuit portion,

wherein said semiconductor island of p-channel thin film transistor has a hole mobility in the range of $10 \text{ cm}^2/\text{V}\cdot\text{sec}$ or more and said semiconductor island of n-channel thin film transistor has an electron mobility in the range of $15 \text{ cm}^2/\text{V}\cdot\text{sec}$ or more,

wherein at least one of said semiconductor islands comprises boron at a concentration in the range of 1×10^{15} to $1 \times 10^{18} \text{ cm}^{-3}$ to control an absolute value of a threshold voltage of said n-channel thin film transistor to be substantially the same as an absolute value of a threshold voltage of said p-channel thin film transistor, and

wherein each of said semiconductor islands has a thickness in the range of 5000 \AA or less.

26. (Amended) A semiconductor circuit having a pixel portion and a shift register, said shift register including at least one pair of complementary p-channel and n-channel thin film transistors, and said pixel portion including at least one thin film transistor, each of said transistors comprising:

a crystalline semiconductor island on an insulating surface, said semiconductor island having source and drain regions and a channel region;

a gate insulating film adjacent to at least said channel region;

a gate electrode adjacent to said gate insulating film; and

a leveling film covering each of said thin film transistors in both of the pixel portion and in the shift register,

wherein said semiconductor island of p-channel thin film transistor has a hole mobility in the range of $10 \text{ cm}^2/\text{V}\cdot\text{sec}$ or more and said semiconductor island of n-channel thin film transistor has an electron mobility in the range of $15 \text{ cm}^2/\text{V}\cdot\text{sec}$ or more,

wherein at least one of said semiconductor islands comprises boron at a concentration in the range of 1×10^{15} to $1 \times 10^{18} \text{ cm}^{-3}$ to control an absolute value of a threshold

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voltage of said n-channel thin film transistor to be substantially the same as an absolute value of a threshold voltage of said p-channel thin film transistor, and

wherein each of said semiconductor islands has a thickness in the range of 5000 Å or less.

C+M
27. (Amended) A semiconductor circuit having a pixel portion and an inverter, said inverter including at least one pair of complementary p-channel and n-channel thin film transistors, and said pixel portion including at least one thin film transistor, each of said transistors comprising:

a crystalline semiconductor island on an insulating surface, said semiconductor island having source and drain regions and a channel region;

a gate insulating film adjacent to at least said channel region;

a gate electrode adjacent to said gate insulating film; and

a leveling film covering each of said thin film transistors in both of the pixel portion and the inverter,

wherein said semiconductor island of p-channel thin film transistor has a hole mobility in the range of 10 cm²/V·sec or more and said semiconductor island of n-channel thin film transistor has an electron mobility in the range of 15 cm²/V·sec or more,

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wherein at least one of said semiconductor islands comprises boron at a concentration in the range of 1×10^{15} to 1×10^{18} cm⁻³ to control an absolute value of a threshold voltage of said n-channel thin film transistor to be substantially same the as an absolute value of a threshold voltage of said p-channel thin film transistor, and

wherein each of said semiconductor islands has a thickness in the range of 5000 Å or less.

C+M
28. (Amended) A semiconductor circuit having a pixel portion and a clocked inverter, said clocked inverter including at least one pair of complementary p-channel and n-channel thin film transistors, and said pixel portion including at least one thin film transistor, each of said transistors comprising:

a crystalline semiconductor island on an insulating surface, said semiconductor island having source and drain regions and a channel region;

a gate insulating film adjacent to at least said channel region;

a gate electrode adjacent to said gate insulating film; and

a leveling film covering each of said thin film transistors in both of the pixel portion and the clocked inverter,

wherein said semiconductor island of p-channel thin film transistor has a hole mobility in the range of $10 \text{ cm}^2/\text{V}\cdot\text{sec}$ or more and said semiconductor island of n-channel thin film transistor has an electron mobility in the range of $15 \text{ cm}^2/\text{V}\cdot\text{sec}$ or more,

wherein at least one of said semiconductor islands comprises boron at a concentration in the range of 1×10^{15} to $1 \times 10^{18} \text{ cm}^{-3}$ to control an absolute value of a threshold voltage of said n-channel thin film transistor to be substantially the same as an absolute value of a threshold voltage of said p-channel thin film transistor, and

wherein each of said semiconductor islands has a thickness in the range of 5000 \AA or less.

29. (Amended) An active matrix display device having a pixel portion and a driver circuit portion, said driver circuit portion including at least one pair of complementary p-channel and n-channel thin film transistors, and said pixel portion including at least one thin film transistor, each of said transistors comprising:

a crystalline semiconductor island on an insulating surface, said semiconductor island having source and drain regions and a channel region;

a gate insulating film adjacent to at least said channel region;

a gate electrode adjacent to said gate insulating film; and

a leveling film covering each of said p-channel and n-channel thin film transistors in both of the pixel portion and a part of the driver circuit portion,

wherein said semiconductor island of p-channel thin film transistor has a hole mobility in the range of $10 \text{ cm}^2/\text{V}\cdot\text{sec}$ or more and said semiconductor island of n-channel thin film transistor has an electron mobility in the range of $15 \text{ cm}^2/\text{V}\cdot\text{sec}$ or more,

wherein at least one of said semiconductor islands comprises boron at a concentration in the range of 1×10^{15} to $1 \times 10^{18} \text{ cm}^{-3}$,

wherein each of said semiconductor islands has a thickness in the range of 5000 \AA or less, and

wherein each of said semiconductor islands comprises oxygen at a concentration not higher than $7 \times 10^{19} \text{ cm}^{-3}$.

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30. (Amended) A semiconductor circuit having a pixel portion and a shift register, said shift register including at least one pair of complementary p-channel and n-channel thin film transistors, and said pixel portion including at least one thin film transistor, each of said transistors comprising:

a crystalline semiconductor island on an insulating surface, said semiconductor island having source and drain regions and a channel region;

a gate insulating film adjacent to at least said channel region;

a gate electrode adjacent to said gate insulating film; and

a leveling film covering each of said thin film transistors in both of the pixel portion and the shift register,

wherein said semiconductor island of p-channel thin film transistor has a hole mobility in the range of $10 \text{ cm}^2/\text{V}\cdot\text{sec}$ or more and said semiconductor island of n-channel thin film transistor has an electron mobility in the range of $15 \text{ cm}^2/\text{V}\cdot\text{sec}$ or more,

wherein at least one of said semiconductor islands comprises boron at a concentration in the range of 1×10^{15} to $1 \times 10^{18} \text{ cm}^{-3}$,

wherein each of said semiconductor islands has a thickness in the range of 5000 \AA or less, and

wherein each of said semiconductor islands comprises oxygen at a concentration not higher than $7 \times 10^{19} \text{ cm}^{-3}$.

31. (Amended) A semiconductor circuit having a pixel portion and an inverter, said inverter including at least one pair of complementary p-channel and n-channel thin film transistors, and said pixel portion including at least one thin film transistor, each of said transistors comprising:

a crystalline semiconductor island on an insulating surface, said semiconductor island having source and drain regions and a channel region;

a gate insulating film adjacent to at least said channel region;

a gate electrode adjacent to said gate insulating film; and

a leveling film covering each of said thin film transistors in both of the pixel portion and the inverter,

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wherein said semiconductor island of p-channel thin film transistor has a hole mobility in the range of $10 \text{ cm}^2/\text{V}\cdot\text{sec}$ or more and said semiconductor island of n-channel thin film transistor has an electron mobility in the range of $15 \text{ cm}^2/\text{V}\cdot\text{sec}$ or more,

wherein at least one of said semiconductor islands comprises boron at a concentration in the range of 1×10^{15} to $1 \times 10^{18} \text{ cm}^{-3}$,

wherein each of said semiconductor islands has a thickness in the range of 5000 \AA or less, and

wherein each of said semiconductor islands comprises oxygen at a concentration not higher than $7 \times 10^{19} \text{ cm}^{-3}$.

32. (Amended) A semiconductor circuit having a pixel portion and a clocked inverter, said clocked inverter including at least one pair of complementary p-channel and n-channel thin film transistors, and said pixel portion including at least one thin film transistor, each of said transistors comprising:

a crystalline semiconductor island on an insulating surface, said semiconductor island having source and drain regions and a channel region;

a gate insulating film adjacent to at least said channel region;

a gate electrode adjacent to said gate insulating film; and

a leveling film covering each of said thin film transistors in both of the pixel portion and the clocked inverter,

wherein said semiconductor island of p-channel thin film transistor has a hole mobility in the range of $10 \text{ cm}^2/\text{V}\cdot\text{sec}$ or more and said semiconductor island of n-channel thin film transistor has an electron mobility in the range of $15 \text{ cm}^2/\text{V}\cdot\text{sec}$ or more,

wherein at least one of said semiconductor islands comprises boron at a concentration in the range of 1×10^{15} to $1 \times 10^{18} \text{ cm}^{-3}$,

wherein each of said semiconductor islands has a thickness in the range of 5000 \AA or less, and

wherein each of said semiconductor islands comprises oxygen at a concentration not higher than $7 \times 10^{19} \text{ cm}^{-3}$.

41. (Amended) An active matrix display device including a pixel portion and a driver circuit portion comprising:

a plurality of pixel electrodes formed on an insulating surface;

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a first plurality of thin film transistors being formed in the pixel portion on said insulating surface and being connected to said pixel electrodes;

a second plurality of thin film transistors being formed in the driver circuit portion on said insulating surface, said second plurality of thin film transistors including at least one pair of complementary p-channel and n-channel thin film transistors; and

a leveling film covering both of the first and second plurality of thin film transistors in the pixel portion and a part of the driver circuit portion,

wherein said second plurality of thin film transistors in said driver circuit include channel semiconductor layers having at least one of an electron mobility $15 \text{ cm}^2/\text{V}\cdot\text{sec}$ or more and a hole mobility of $10 \text{ cm}^2/\text{V}\cdot\text{sec}$ or more,

wherein each of the channel semiconductor layers comprises boron at a concentration in the range of 1×10^{15} to $1 \times 10^{18} \text{ cm}^{-3}$, and

wherein each of said channel semiconductor layers has a thickness of 5000 \AA or less.

43. (Amended) A device according to claim 41 wherein said semiconductor is silicon.

44. (Amended) A device according to claim 41 wherein each of the first and second plurality of said thin film transistors comprises a gate electrode formed over said channel semiconductor layers having a gate insulating film therebetween.

48. (Amended) A device according to claim 41 wherein said channel semiconductor layers exhibit a Raman peak shifted to a lower frequency side from 522 cm^{-1} .

55. (Amended) A device according to any one of claims 21, 25, and 29 wherein said source and drain regions of n-channel thin film transistor are introduced with phosphorus at a dose of 1×10^{15} to $5 \times 10^{15} \text{ cm}^{-2}$.

59. (Amended) A device according to any one of claims 21, 25, 29, and 41, wherein said leveling film comprises an organic resin.

61. (Amended) A circuit according to any one of claims 22-24, 26-28, and 30-32, wherein said semiconductor island of p-channel thin film transistor has a hole mobility in the range of $200 \text{ cm}^2/\text{V}\cdot\text{sec}$ or less and said semiconductor island of n-channel thin film transistor has a electron mobility in the range of $300 \text{ cm}^2/\text{V}\cdot\text{sec}$ or less.

62. (Amended) A device according to any one of claims 21, 25, and 29, wherein said semiconductor island of p-channel thin film transistor has a hole mobility in the range of 200

cont, $\text{cm}^2/\text{V}\cdot\text{sec}$ or less and said semiconductor island of n-channel thin film transistor has a electron
B6 mobility in the range of $300 \text{ cm}^2/\text{V}\cdot\text{sec}$ or less.

B7 63. (Amended) A device according to claim 41, wherein said second plurality of thin
film transistors in said driver circuit include channel semiconductor layers having at least one of
an electron mobility $300 \text{ cm}^2/\text{V}\cdot\text{sec}$ or less and a hole mobility of $200 \text{ cm}^2/\text{V}\cdot\text{sec}$ or less.
